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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/665,171

09/19/2003

Rodney E. Hooker

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6328

23669

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09/18/2006

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EXAMINER

PATEL, HETUL B

ART UNIT

PAPER NUMBER

2186

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/665,171		HOOKER, RODNEY E.	
	Examiner		Art Unit	
	Hetul Patel		2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 and 32-46 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 and 32-46 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>06/24/2006</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is responsive to communication filed on July 12, 2006. The assertion of non-compliance is removed; and the amendment filed on June 15, 2006 has been entered and carefully considered.
2. Claims 17-31 are cancelled and claims 1, 32-35 and 41-43 are amended.
3. The IDS filed on 06/24/2006 has been received and carefully considered.
4. Applicant's arguments filed on June 15, 2006 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-16 and 32-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Kyker et al. (USPN: 6,594,734) hereinafter, Kyker.

As per claim 1, Kyker teaches an apparatus in a pipeline microprocessor (i.e. 301A in Fig. 4A), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising: instruction cache management logic (i.e. 415 in Fig. 4A), configured to receive an address corresponding to a next instruction to

be fetched (i.e. the physical address received by the ITLB), and configured to detect that a part of a memory page corresponding to said next instruction cannot be freely accessed without checking for coherency of the instructions within said part of said memory page (i.e. the physical addresses stored in ITLB) and, upon detection, configured to provide said address; and synchronization logic, configured to receive said address from said instruction cache management logic, and configured to direct data cache management logic to check for coherency of the instructions within said part of said memory page, and, if the instructions are not coherent within said part of said memory page, said synchronization logic is configured to direct the pipeline microprocessor to stall a fetch of said next instruction until the stages of the pipeline microprocessor have executed all preceding instructions (e.g. see the abstract, claim 17 and Fig. 4A).

As per claim 32, Kyker teaches a method in a pipeline microprocessor (i.e. 301 in Fig. 4A), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising: within instruction cache (i.e. 414A in Fig. 4A), detecting that a part of a memory page corresponding to a next instruction to be fetched cannot be freely accessed without checking for coherency of the instructions within the part of the memory page; directing logic within a data cache to check for coherency of the instructions within the part of the memory page; and if the instructions are not coherent, stalling a fetch of the next instruction from the instruction cache until the stages of the pipeline microprocessor have executed all preceding instructions (e.g. see the abstract, claim 17 and Fig. 4A).

As per claim 2, Kyker teaches the claimed invention as described above and furthermore, Kyker discloses that when a snoop is triggered, the physical address of the store into memory is provided to the snoop port and the ITLB performs a comparison with all the physical page addresses located within the ITLB 412 to determine whether a store into memory has addressed a page which may be stored in the instruction cache 414A. If a match is found, a store occurred into memory within a page of instructions that may be stored within an instruction cache and the cache and the instruction pipeline may be incoherent with memory (e.g. see Col. 7, lines 6-15). In other words, Kyker does teach that the instruction cache management logic evaluates an instruction translation lookaside buffer (ITLB) entry corresponding to said address to detect that said part cannot be freely accessed, as claimed.

As per claim 3, Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the ITLB entry corresponds to the memory page (e.g. see claim 17).

As per claim 4, Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the ITLB entry comprises a plurality of part-page ownership bits (i.e. FINE HITS bits) (e.g. see Col. 11, line 59+).

As per claims 5 and 6, Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that one of said plurality of part-page ownership bits (i.e. one of the FINE HITS bits) corresponds to the part of said memory page (i.e. the smaller block of memory within a memory page) and remaining ones of said plurality of

part-page ownership bits correspond to remaining parts of said memory page (e.g. see Col. 11, line 59+).

As per claims 7 and 8, Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the part can be freely accessed if said one of said plurality of part-page ownership bits is set; and the part cannot be freely accessed if said one of said plurality of part-page ownership bits is not set (i.e. "[T]he ITLB 412 and associated snoop logic illustrated in FIG. 6 only indicate an SMC hit if a physical match has occurred") (e.g. see Col. 11, line 59+).

As per claim 9, Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the plurality of part-page ownership bits comprise four part-page ownership bits, and wherein said part comprises one-quarter of said memory page (i.e. "[T]he FINE HIT bits for simplicity are selected in the preferred embodiment to provide a granularity of 1K or 1024 addresses within a 4K page of memory. While this is the size utilized in the preferred embodiment, other granularities may be utilized. In the preferred embodiment, the ITLB 412 includes four FINE HIT bits with each line of translation contained therein, each being associated with a 1K block of addresses within a 4K page. ") (e.g. see Col. 11, line 59+).

As per claims 10-16, Kyker teaches the claimed invention as described above and furthermore, Kyker teaches about evaluating ITLB entry corresponding to the address to detect that the instruction is not coherent within the part of the memory page; the ITLB entry comprises a plurality for part-page ownership bits, each corresponds to the part of the memory page; if one of said plurality for part-page ownership bits is set,

the corresponding part cannot be freely accessed, as recited in rejection of claims 2-9 above. Claims 10-16 are claiming similar limitations as claims 2-9 except DTLB instead of ITLB. Since Kyker discloses that "[T]he present invention has been described herein with reference to instructions in an instruction translation lookaside buffer (ITLB) and an instruction cache, but it is equally applicable for cache coherency between memory and a cache storing data where a translation lookaside buffer is used" (e.g. see Col. 14, lines 16+), Kyker also teaches the limitations of claims 10-16. Based on this rationale, claims 10-16 are rejected.

As per claims 41-46, 40 and 33-39, see arguments with respect to the rejection of claims 2-16, respectively. Claims 41-46, 40 and 33-39 are also rejected based on the same rationale as the rejection of claims 2-16, respectively.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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